

# MIMOSA

## Microsystems platform for Mobile Services and Applications

**FP6 Contract: IST-2002-507045**

---



### **WP4 – System Integration**

#### **Deliverable report**

Deliverable ID:	<b>D4.6</b>
Deliverable Title:	<b>Development and integration of thick SOI resonators</b>
Responsible partner:	VTT
Contributors:	VTT

#### PROPRIETARY RIGHTS STATEMENT

This document contains information, which is proprietary to the MIMOSA Consortium. Neither this document nor the information contained herein shall be used, duplicated or communicated by any means to any third party, in whole or in parts, except with prior written consent of the MIMOSA consortium.

## Document Information

**Document Name:** Development and integration of thick SOI resonators  
**Document ID:** MIMOSA-WP4-D4.6  
**Revision:** Final  
**Revision Date:** 28.9.2005  
**Author:** Panu Pekko  
**Security:** PUBLIC (PU)

## Approvals

	Name	Company	Date	Visa
<i>Technical Coordinator</i>	Pascal ANCEY	ST Fr	03/11/05	OK
<i>WP leader</i>	Xavier GAGNARD	ST Fr	17/10/05	OK
<i>Quality Manager</i>	Cédric ROBET	ALMA	17/10/05	OK

## Documents history

Revision	Date	Modification	Author
V0	17/10/05	Creation	P. PEKKO
Vfinal	29/11/05	Correction in the title (front page)	C. ROBET

## Content

<b>INTRODUCTION</b>	<b>4</b>
<b>THICK SOI (10 <math>\mu</math>M) RESONATORS</b>	<b>4</b>
<b>PLUG-UP METHOD</b>	<b>5</b>
<b>FABRICATED STRUCTURES</b>	<b>6</b>
<b>PROCESS DESCRIPTION</b>	<b>7</b>
<b>RESULTS</b>	<b>7</b>
<b>CONCLUSIONS, FUTURE WORK</b>	<b>12</b>

## INTRODUCTION

WP4 focuses in microsystem integration. Essential part of it is the monolithic integration of MEMS and CMOS. The objective of the work reported is to demonstrate the suitability of plug-up –method in fabrication of MEMS resonator with electronic circuitry on the same chip.

The deliverable contains:

- The description of thick SOI resonators
- The description of Plug-up method enabling the monolithical integration
- List of structures included to the design
- General description of fabrication process
- Results of device characterization
- Conclusions and discussion

## THICK SOI (10 $\mu\text{m}$ ) RESONATORS

MEMS resonators offer several possible advances compared to conventional quartz crystal. These include e.g. smaller size, integrability with IC electronics and low power consumption. VTT has developed a square shaped 13.1 MHz MEMS resonator based on square-extensional vibration mode, i.e. vibration mode where square plate is zooming in and out preserving its original shape. Figure 1 shows a SEM (scanning electron microscope) image of the resonator. The quality factor  $Q$  of device approaches 200 000 and the maximum drive level reaches 0.12 mW. When the resonator was connected to oscillator circuitry the phase noise reached the world-record level, fulfilling the GSM-specification (-130 dBc/Hz@1 kHz).

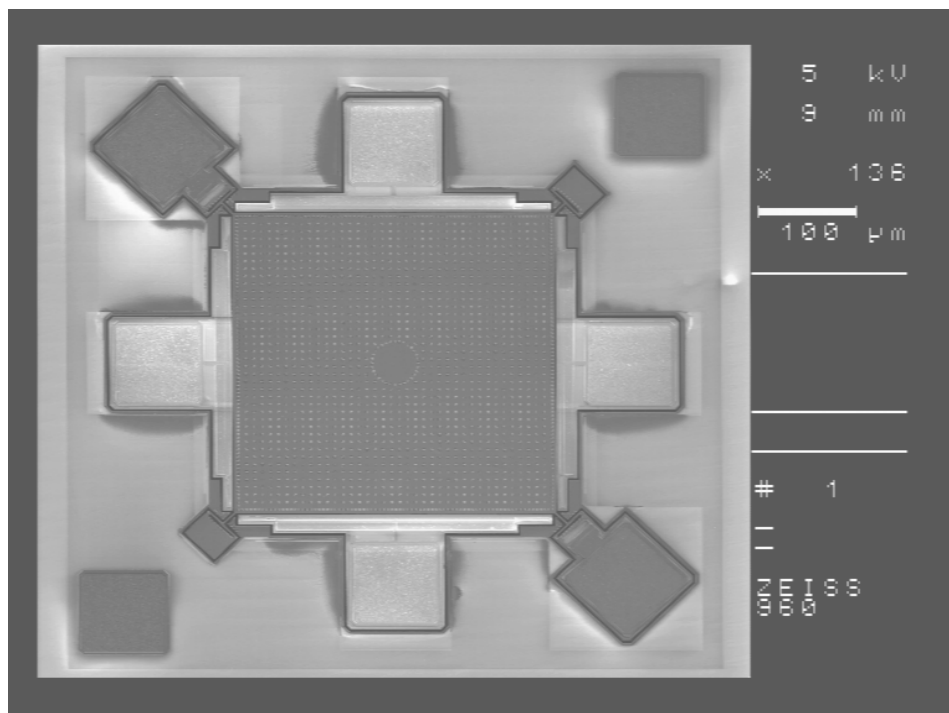


Figure 1. Square-extensional thick SOI MEMS resonator

The resonators have been fabricated on 10  $\mu\text{m}$  thick SOI layer. Within Mimosa stand-alone resonators have been fabricated both with ‘traditional’ technology and plug-up method. In traditional method the resonator plate is perforated with holes and these holes will be utilized in release etching of vibrating structure. The plug-up –method will be described more thoroughly in next chapter.

## PLUG-UP METHOD

Plug-up method is a novel fabrication technology developed at VTT. It enables the monolithic integration of MEMS and CMOS structures on same chip. A schematic picture of plug-up –process is presented in Fig. 2.

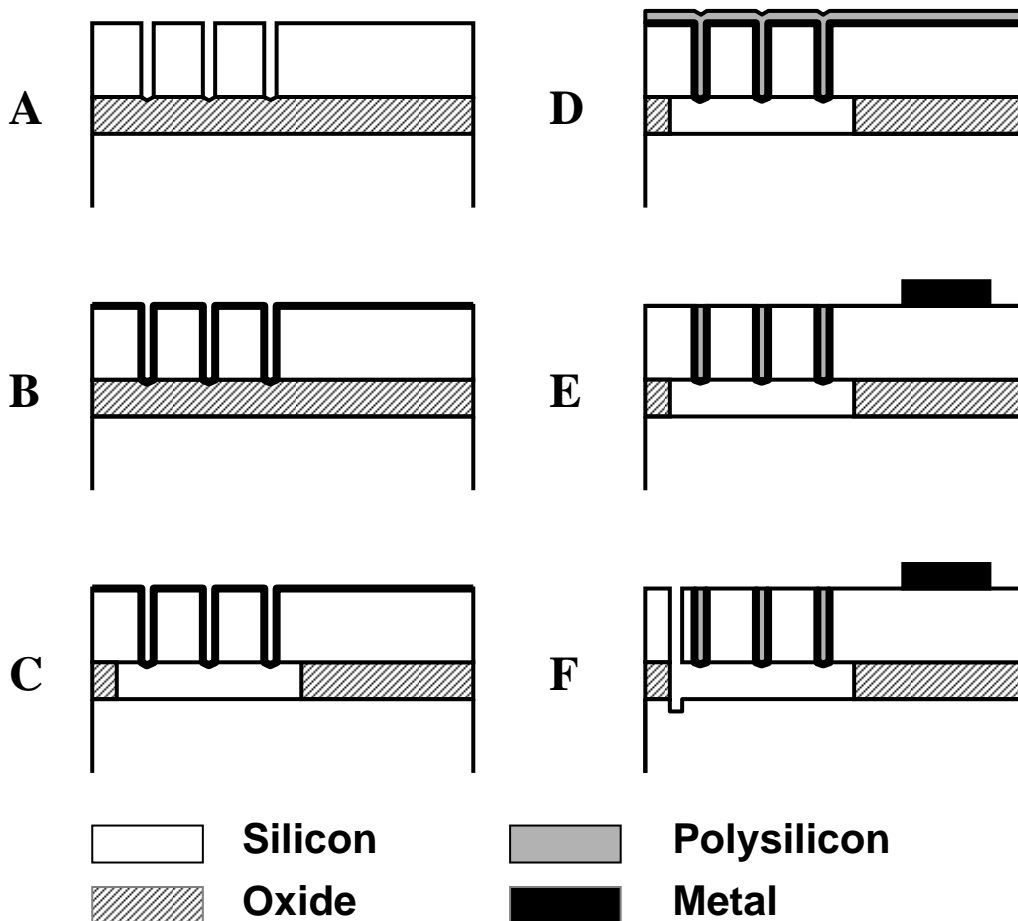


Figure 2: Cross-section of the Plug-up process: A) DRIE (Deep Reactive Ion Etching) of etch access holes, B) deposition of semipermeable polysilicon layer, C) sacrificial layer etching and release drying, D) refilling of holes with polysilicon plugs, E) polysilicon etchback, F) back-end processes: e.g. CMOS fabrication and optional opening of structures by DRIE.

The process sequence is as follows. First, arrays of small holes are etched through deposited etch stop layer and the SOI structure layer (several microns thick) in

regions where the cavities will be formed. Then, after photoresist etch mask removal and cleaning, a thin semipermeable layer of polysilicon is conformally deposited over the surface. The sacrificial layer (the SOI buried oxide) is etched with HF through the pinholes in the thin polysilicon film. If formation of the anti-stiction dimples is desired, a short, timed wet oxide etch step is performed prior to the deposition of the semipermeable polysilicon film. After the sacrificial etching and rinsing steps, the wafer is dried using supercritical carbon dioxide. The holes in the structure layer are then refilled to form plugs using a selected vacuum deposition method, typically low pressure chemical vapor deposited (LPCVD) polysilicon is used. At this point the etch result can be checked using near infrared microscopy to verify that the etch length is correct. The polysilicon plugs planarize the surface and close up the cavities. Practically no deposition occurs through the small holes in polysilicon and the inside of the cavities remains clean. After closing the structure, the top surface films are removed - excluding the plugs – and a clean, planar, single crystal surface is revealed. The pressure inside the cavity remains in the pressure range of the deposition process.

After the single crystal surface is revealed, e.g. standard CMOS process or metal conductor patterning can be performed. As the wafer surface is planarized, there is no need for difficult lithographic patterning over high topographic steps. A wide variety of metals or other films can be deposited and patterned on this surface, because the wafer does not need to be exposed to HF anymore. As a final process step (Fig. 2F), the structure layer can be patterned and etched into desired shape either leaving the cavities in vacuum or by etching them to form for example resonators. The polysilicon plugs constitute a minor portion of the structural material and the mechanical properties of the devices are determined mainly by the single crystal structure layer, which typically has very low internal stress allowing fabrication of complex MEMS devices. The maximum deflection of the structure should be limited to the thickness of the buried oxide to avoid touching of the structure to the substrate.

As a conclusion, the Plug-up –method has e.g. the following benefits:

- 1) Because the cavities are formed prior to metal connectors, the metals are not exposed to sacrificial layer etchants
- 2) Because the wafer surface is planarized after the cavity formation, there are no high topography steps on the wafer exacerbating the device fabrication
- 3) The antistiction structures can easily be fabricated on MEMS device without extra lithography steps
- 4) If the cavities are opened (as in resonator fabrication), the notching is not a problem in DRIE etching due to the absence of insulating etch-stop layer

These features enable the use of Plug-up –method as a tool of monolithical integration. In MimosA it has been used to fabrication of stand-alone resonators and to monolithical integration of resonators and CMOS circuitry.

## FABRICATED STRUCTURES

Several structures were fabricated on test wafers, e.g.:

- Stand-alone resonators (13.6 MHz)
- Charge pumps
- Bipolar transistors
- MOS-transistors
- Buffer amplifiers

Stand-alone components were used to evaluate the quality of MEMS and CMOS fabrication.

## PROCESS DESCRIPTION

The fabrication process used was combination of plug-up process and standard CMOS process (see Fig. 2). An additional feature of the process was the manufacturing of oxide bridges. These bridges were used by metal connectors between MEMS and CMOS parts. The schematic cross-section of fabricated structure is shown in Fig. 3.

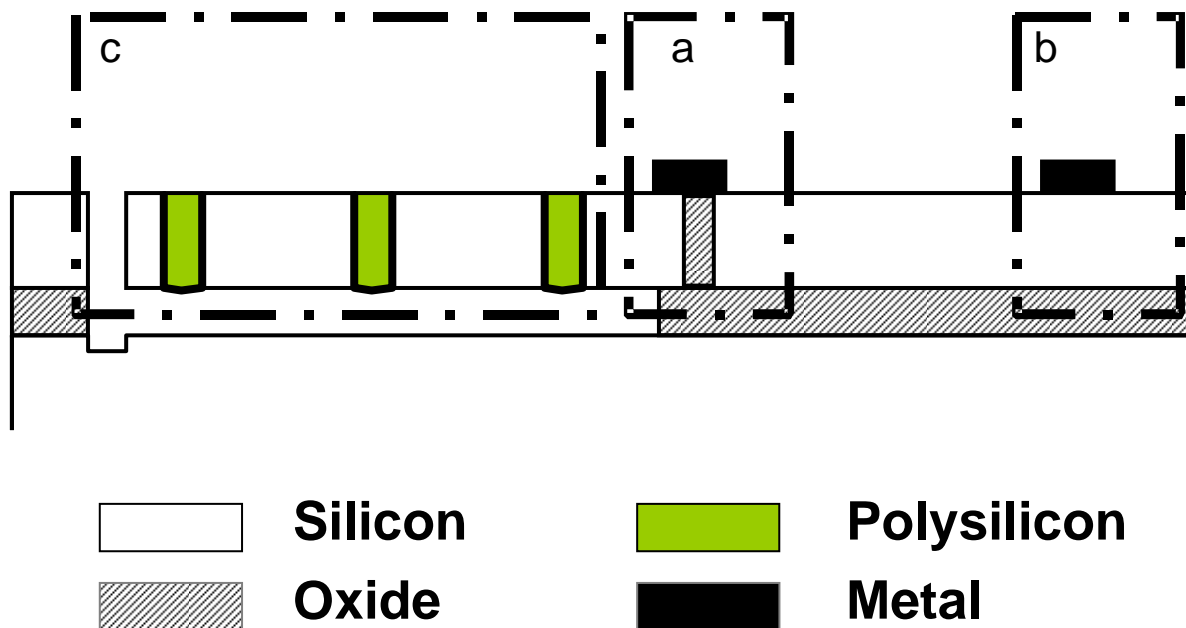


Figure 3. Schematic cross-section of fabricated structure. Oxide bridge is marked with letter 'a', CMOS part with 'b' and MEMS part with 'c'.

## RESULTS

The monolithical integration of buffer amplifier and MEMS resonator was successful. The transmission response measurements indicated that both the resonator and CMOS circuitry were functional. Gain measurement curves of resonator-buffer amplifier combination are shown in Fig. 4 (amplitude). The resonance frequency is

around 13.596 MHz. With increasing bias voltage the resonance frequency moves to lower frequencies.

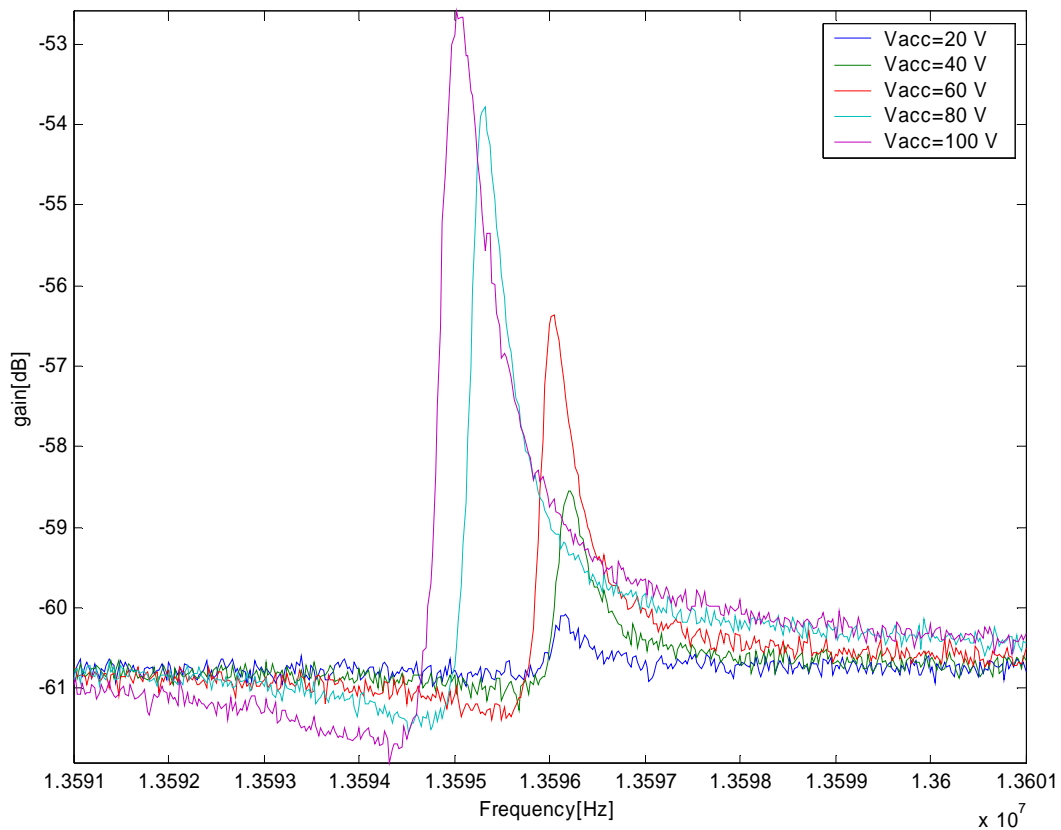


Fig. 4. Gain measurement curves of monolithically integrated buffer amplifier-MEMS resonator –system.

In Figure 5 is shown an optical microscope image of fabricated buffer amplifier circuitry and MEMS resonator. The CMOS part has been isolated from MEMS part with air gap except in locations where connectors were formed. In those places oxide isolation was used.

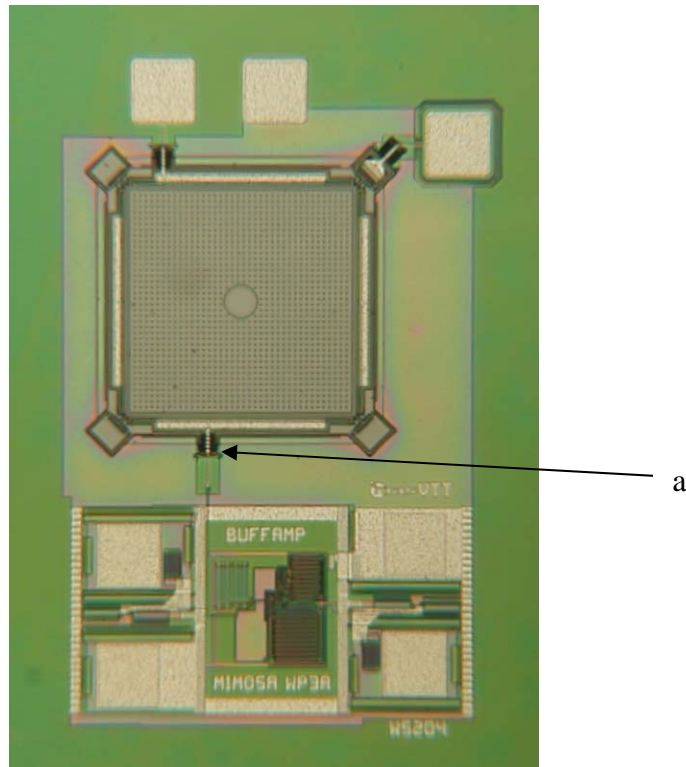


Figure 5. Buffer amplifier with monolithically integrated MEMS resonator. The oxide bridge isolating MEMS part and CMOS part is marked with letter 'a'.

In figure 6 is shown the measured transmission response of stand-alone resonator.

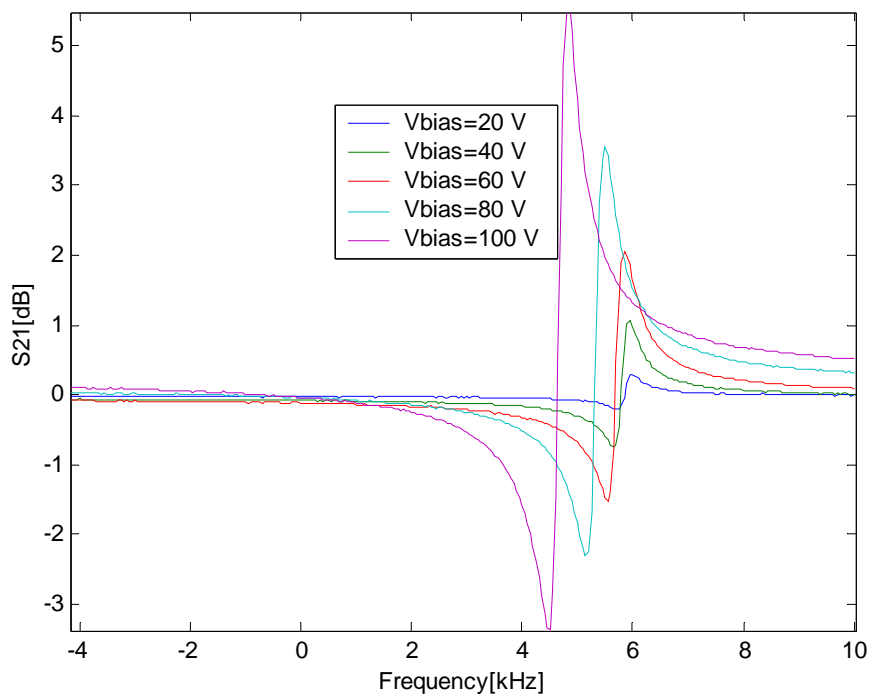


Figure 6. Measured transmission response of stand-alone resonators. The resonance frequency is around 13.596 MHz.

In the devices there are still some features to be optimized. Three unexpected results were observed:

- 1) In the first fabricated devices some leakage current was observed over the oxide bridges used to isolate MEMS and CMOS.
- 2) The resonance peak was asymmetric, i.e. the peak above zero level is stronger than the one below zero level.
- 3) Close-up of the resonance showed that resonance was not 'clean' but showed 'jitter'. This is presented in Fig. 7.

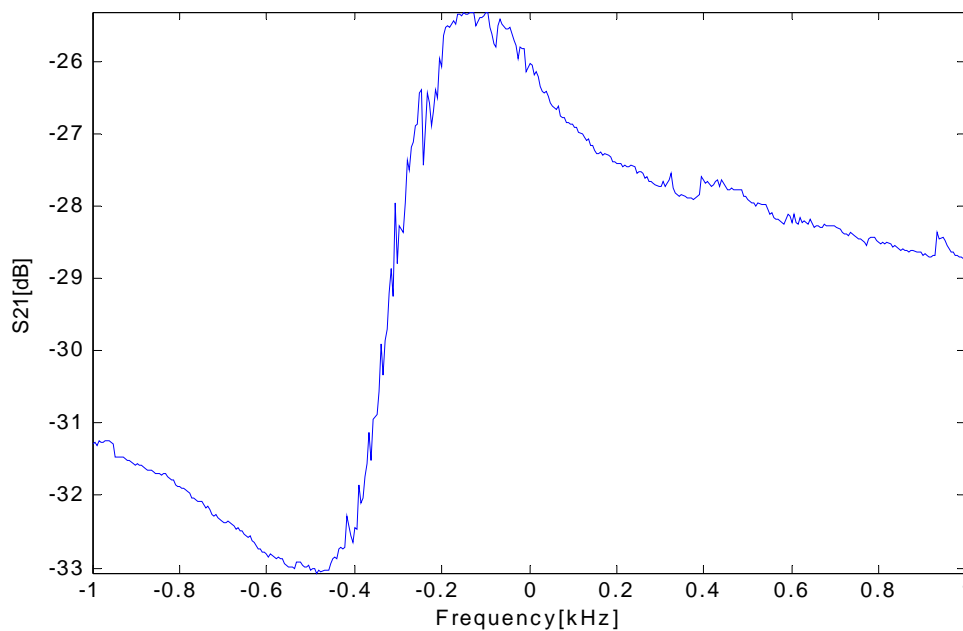


Figure 7. Close-up of stand-alone device resonance.

An oxide bridge structure is shown in Fig. 5 and marked with letter 'a'. It was estimated that the origin of leakage was residual silicon on oxide bridge walls although in principle the silicon surrounding the oxide bridge structure should be removed in the final resonator-forming deep etching step. The reason to existence of residuals is that the final DRIE step is optimized to produce as narrow high aspect ratio gap as possible. This also means that the mask undercut in etching process is minimized and etch profile verticality maximized. Consequently, if the oxide bridge wall profile is even faintly positive (V-shaped) the etching will be shadowed by upper part of oxide bridge and residuals will stay on the bridge walls.

To overcome this problem the final deep etching step was divided to two phases. In the first phase only the surroundings of oxide bridges were etched with the recipe that normally creates a small undercut below the etching mask. It was expected that this would remove possible residuals. After that the narrow gaps were etched in the second phase. The measurements performed after the procedure showed that the leakage current was disappeared. This confirmed the role of silicon residuals. The future objective is to develop the oxide bridge manufacturing process so that two-phase deep etching would not be needed.

The reason to asymmetry in resonance curves is still unclear and under investigation. At the moment it seems that the reason is not of mechanical origin (i.e. caused by MEMS structure).

The reason to 'jitter' in resonance curve is most likely the particles in the gaps. This hypothesis is supported by SEM images of incompletely etched polysilicon plugs (Fig. 8). The center areas of plugs have become etched but a sleeve-like structure has resisted etching. If a sleeve structure breaks the result is probably particles in the gap. The reason to incomplete etching is not known at the moment but a possible reason is e.g. the equipment failure in polysilicon deposition. In the future the problem can be avoided by placing the plugs outside the area which will be deep etched. The process development will also be performed to find out the original reason.

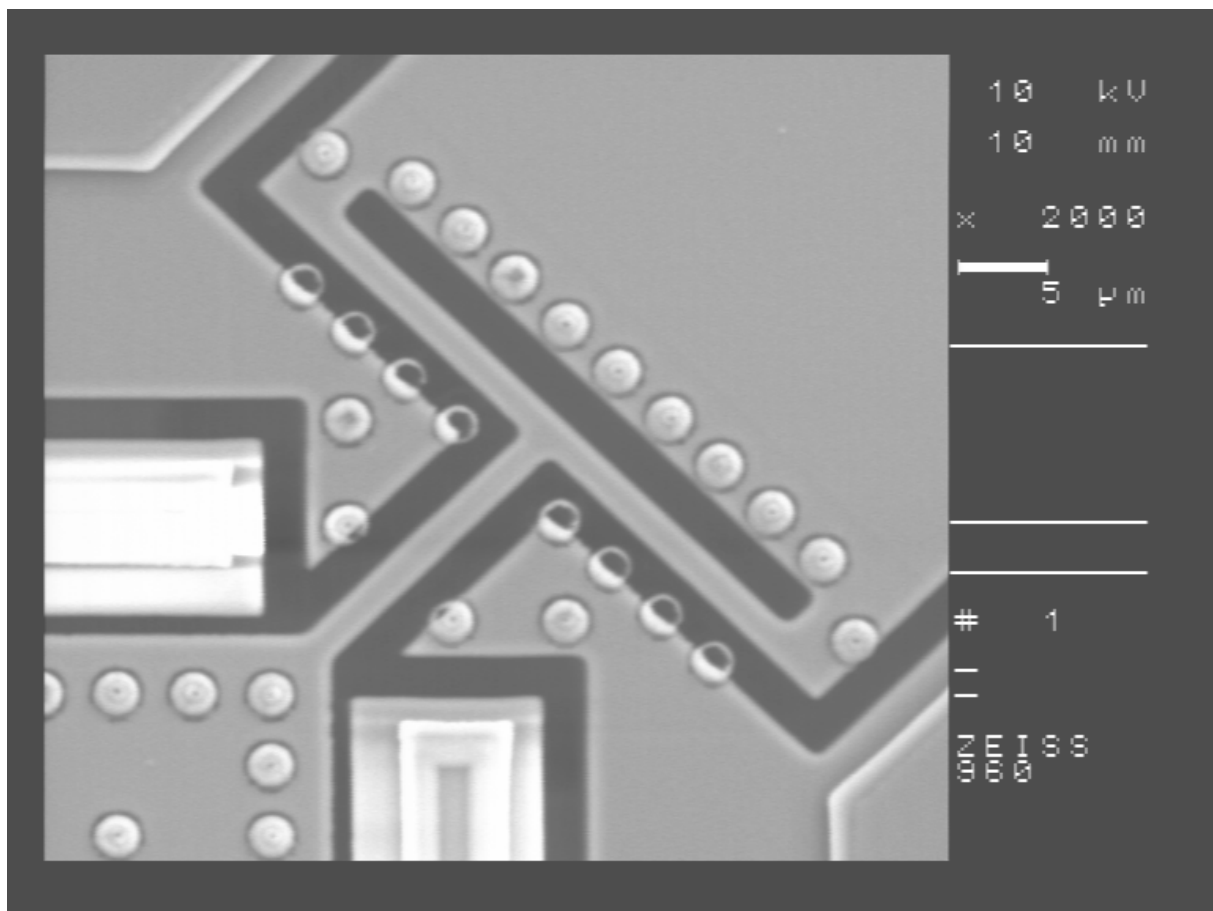


Figure 8. SEM image of incompletely etched polysilicon plugs.

Despite of these problems the resonators worked well enough to demonstrate the integration potential.

The CMOS part of processed wafers worked as expected. The test structure measurements indicated that devices were functional.

## CONCLUSIONS, FUTURE WORK

The objective of the work was to integrate MEMS structure monolithically to electronic circuitry. This goal was reached and the suitability of plug-up –process was demonstrated.

Concerning the integration technology presented in this work, there is some fine tuning to do. E.g. the reason to incomplete etching of polysilicon plugs must be investigated.

Concerning the resonator integration specifically, there are also some challenges. The electrode gap width must be reduced to decrease the demanded bias voltage levels. This would enable the fabrication of oscillator chips. This work will be continued already in the Mimosa project and will be the main objective during the last phase of the project. Another task is the packaging of device. For the resonator to be functional, a vacuum ( $p < 1$  mbar) package is demanded. One possible solution is the packaging technology developed by Fhg-Isit in Mimosa project.